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NEXT VISION DISPLAY

SPECIFICATION

CUSTOMER : _____

MODULE NO.: NE037-N001GD

Version	1.0
Engineer	
Date	2022/06/16

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Customer:
Approved by

NEXT VISION DISPLAY CO., LTD.

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Overview

Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white full display capabilities. The 3.7 inch active area contains 240×416 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

Features

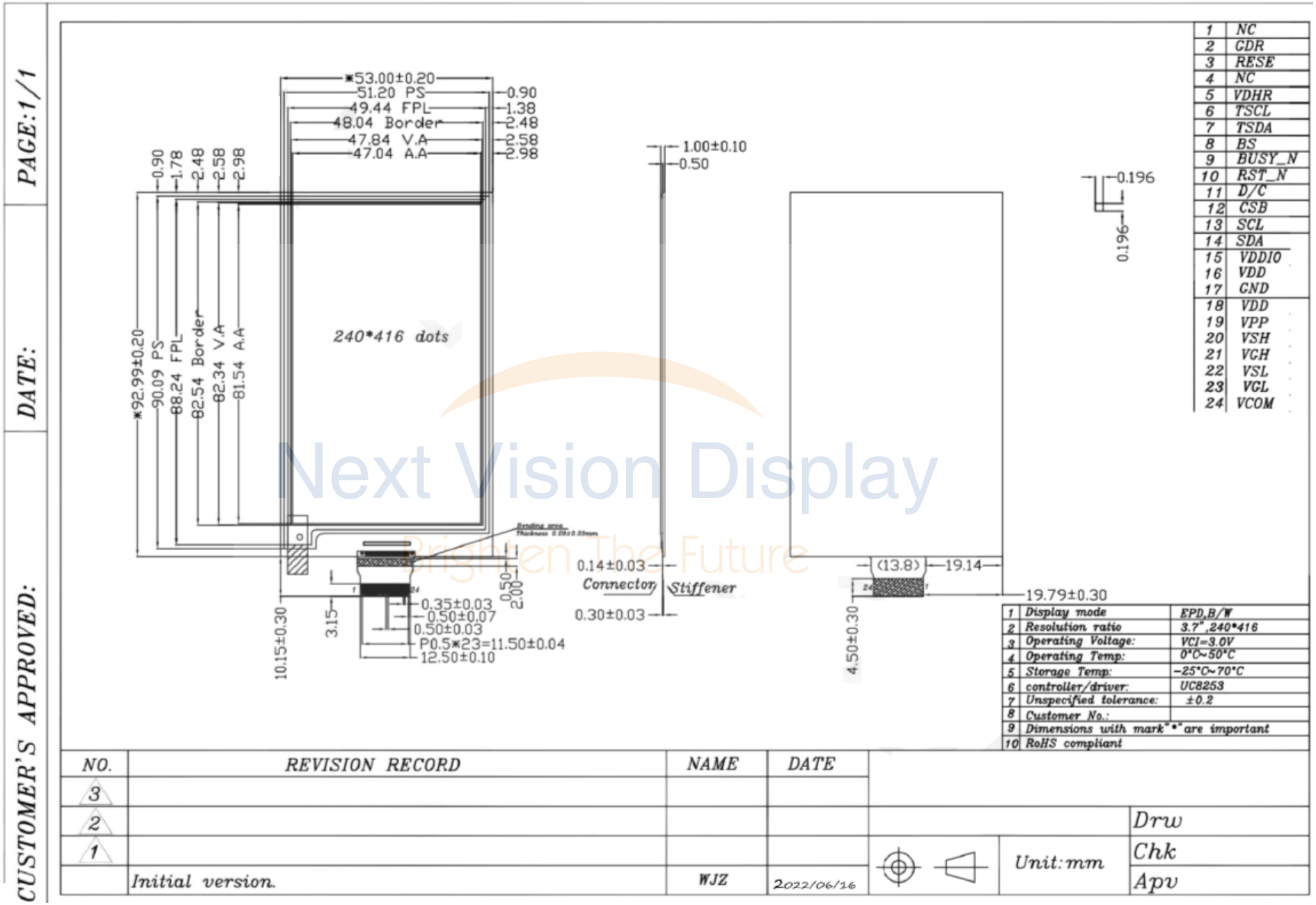
- 240×416 pixels display
- High contrast High reflectance
- Ultra wide viewing angle Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform can stored in On-chip or written by MCU
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor
- Built-in temperature sensor

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Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	3.7	Inch	
Display Resolution	240(H)×416(V)	Pixel	Dpi:130
Active Area	47.04×81.54	mm	
Pixel Pitch	0.196×0.196	mm	
Pixel Configuration	Square		
Outline Dimension	53(H)×92.99(V) ×1.0(D)	mm	
Weight	9.1±0.05	g	

Mechanical Drawing of EPD module



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Input /Output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	TSCL	O	I^2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I^2C Interface to digital temperature sensor Da a pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
1	VPP	P	FOR TEST	
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

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I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be inte preted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, th eration of chip should not be interrupted, command should not be sent. The chip w put Busy pin High when -Outputting display waveform -Communicating with dig al temperature sensor.

Note 5-5: Bus interface selection pin

BS1 State	MCU In erface
L	4-lines serial peripheria interface(SPI) - 8 bits SPI
H	3- lines serial peripherial interface(SPI) - 9 bits SPI

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Electrical Characteristics

Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.3 to +6.0	V
Logic Input voltage	VIN	-0.3 to VCI +0.3	V
Operating Temp range	TOPR	0 to +50-	ºC
Storage Temp range	TSTG	25 to+70	ºC
Optimal Storage Temp	TSTGo	23±2	ºC
Optimal Storage Humidity	HSTGo	55±10	%RH

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

7.2. Display DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0 R =23ºC

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{CI}	-	VCI	2.3	3.0	3.6	V
Core logic voltage	V_{DD}		VDD	2.3	3.0	3.6	V
High level input voltage	V_{IH}	-	-	0.8 V_{CI}	-	V_{CI}	V
Low level input voltage	V_{IL}	-	-	0	-	0.2 V_{CI}	V
High level output voltage	V_{OH}	I_{OH}= 400uA	-	0.8 VCI	-	V_{CI}	V
Low level output voltage	V_{OL}	I_{OL}=- 400uA	-	0	-	0.2 V_{CI}	V
Typical power	P_{TYP}	V_{CI}=3.0V	-	-	TBD	-	mW
Deep sleep mode	P_{STPY}	V_{CI}=3.0V	-	-	0.003	-	mW
Typical operating current	Iopr_V_{CI}	V_{CI}=3.0V	-	-	TBD	-	mA
Full update time	-	25 ℃	-	-	3	-	sec
Fast update time	-	25 ℃	-	-	1	-	sec
Sleep mode current	Islp_V_{CI}	DC/ DC off No clock No input load Ram data retain	-	-	25		uA
Deep sleep mode current	Idslp_V_{CI}	DC/ DC off No clock No input load Ram data not retain	-	-	1	5	uA

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Notes:
1) Refresh time: the time it takes for the whole process from the screen change to the screen stabilization.
2) The difference between different refresh methods:
Full refresh: The screen will flicker several times during the refresh process;
Fast Refresh: The screen will flash once during the refresh process.

During the fast refresh or partial refresh of the electronic paper, it is recommended to add a full-screen refresh after 5 consecutive operations to reduce the accumulation of afterimages on the screen.

1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.

2. The deep sleep power is the consumed power when the panel cont oller is in deep sleep mode.

3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display.

Panel AC Characteristic

MCU Interface

UC8253 provides 3-wire/4-wire serial inte ce for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at teh clock rising edge. When too many parameters are input, the chip accepts only def ed parameters, and ignores undefined ones.

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MCU Serrial Interface (4-wire SPI)

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH eve y 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

Interface Timing

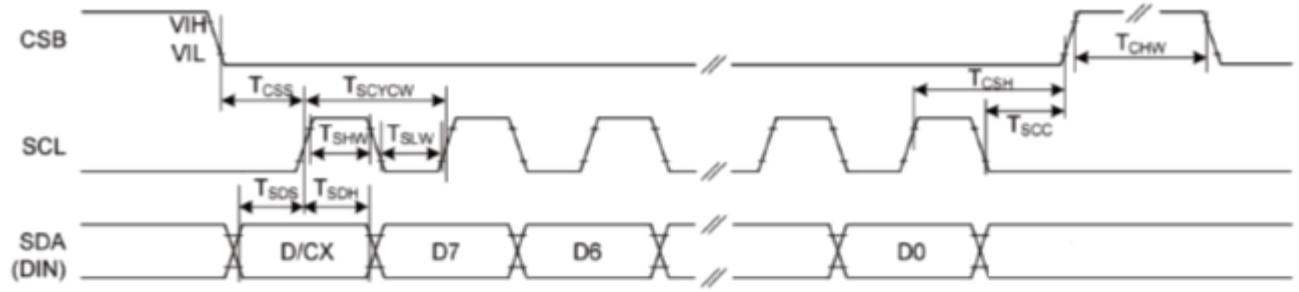


Figure: 3-wire Serial Interface Characteristics (Write mode)

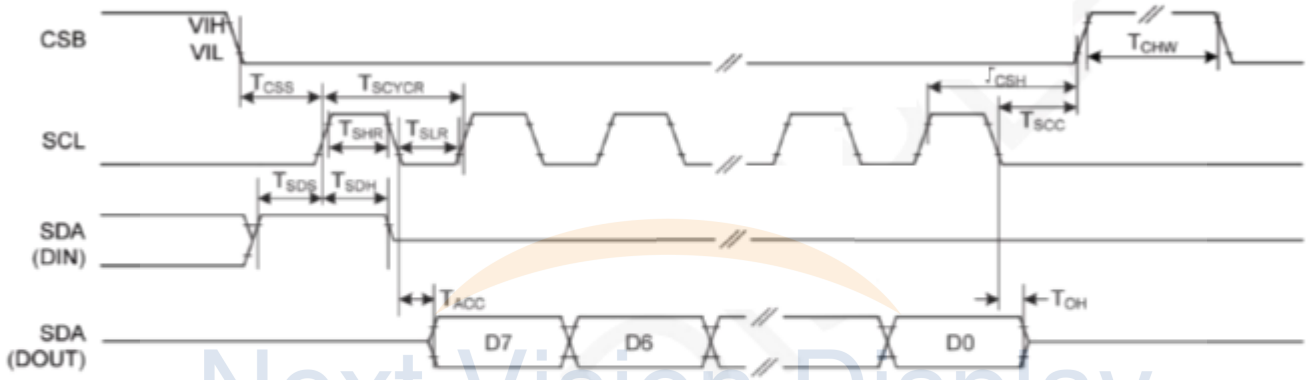


Figure: 3-wire Serial Interface Characteristics (Read mode)

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Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL "H" pulse width (Write)	35			ns
T_{SLW}		SCL "L" pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	350			ns
T_{SHR}		SCL "H" pulse width (Read)	175			ns
T_{SLR}		SCL "L" pulse width (Read)	175			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			250	ns
T_{OH}		Output disable time	15			ns

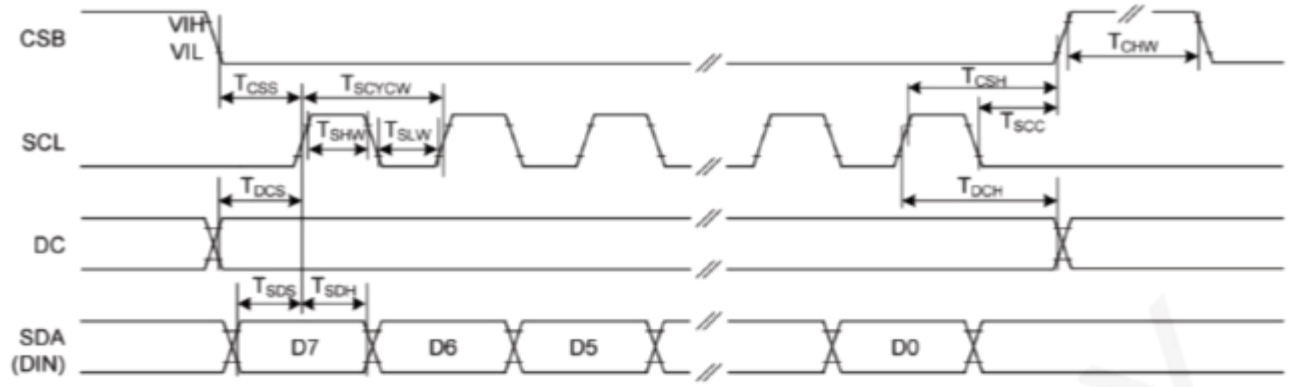


Figure: 4-wire Serial Interface Characteristics (Write mode)

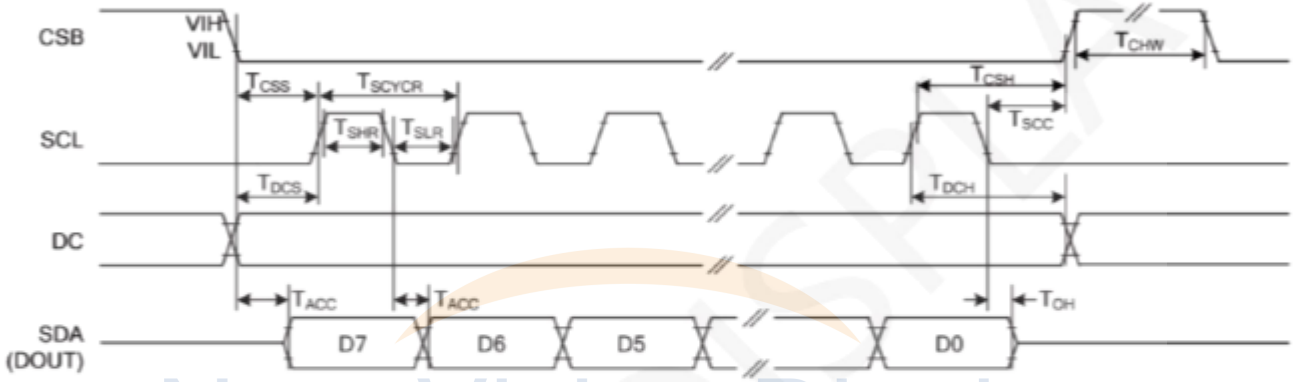


Figure: 4-wire Serial Interface Characteristics (Read mode)

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Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL "H" pulse width (Write)	35			ns
T_{SLW}		SCL "L" pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	350			ns
T_{SHR}		SCL "H" pulse width (Read)	175			ns
T_{SLR}		SCL "L" pulse width (Read)	175			ns
T_{DCS}	DC	DC setup time	30			ns
T_{DCH}		DC hold time	30			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			250	ns
T_{OH}		Output disable time	15			ns

Optical Specifications

. Specification

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	Indoor	8:1		-		8-2
GN	2Grey Level	-		DS+(WS-DS)*n(m-1)			8-3
T update	Image update time	at 25 °C		3		sec	
Life		Topr		1000000times or 5years			

Notes:

8-1. Luminance meter: Eye-One Pro Spectrophotometer.

8-2. CR=Surface Reflectance with all white pixel/Surface ctance with all black pixels.

8-3. WS: White state, DS: Dark state

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