Winstar Display Co., LTD
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SPECIFICATION

CUSTOMER ： _____

MODULE NO.: WO12864-84IC2#030-FC

General Specification

Item	Dimension	Unit
Number of Characters	128 x 64 dots	—
Module dimension	55.2x 39.8 x 7.8(MAX)	mm
View area	45.2 x 27.0	mm
Active area	40.92 x 24.28	mm
Dot size	0.28 x 0.34	mm
Dot pitch	0.32 x 0.38	mm
LCD type	STN Negative, Blue Transmissive, (In LCD production, It will occur slightly color difference. We can only guarantee the same color in the same batch.)	
Duty	1/64 , 1/9 Bias	
View direction	6 o'clock	
Backlight Type	LED White	

first FC components
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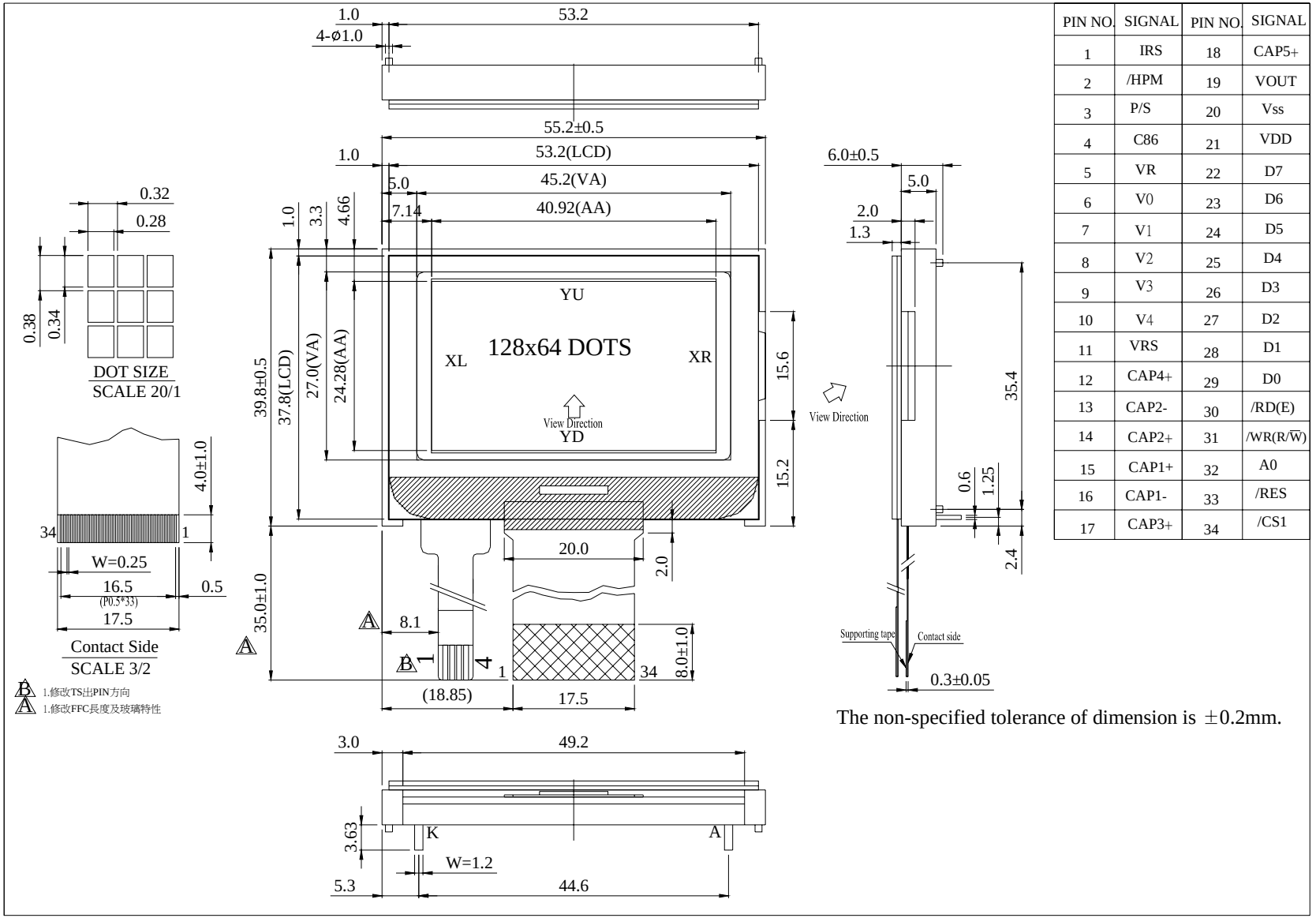
Interface Pin Function

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Level</th><th>Description</th></tr>
<tr><td>1</td><td>IRS</td><td></td><td>This terminal selects the resistors for the V5 voltage level adjustment.
IRS = “H”: Use the internal resistors.
IRS = “L”: Do not use the internal resistors.
The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal. This pin is enabled only when the master operation mode is selected. It is fixed to either “H”or
“L” when the slave operation mode is selected.</td></tr>
<tr><td>2</td><td>/HPM</td><td></td><td>This is the power cpntrol terminal for the power supply circuit for liquid crystal drive.
HPM=”H”:Normal made
HPM=”L”:High power mod</td></tr>
<tr><td>3</td><td>P/S</td><td></td><td>This is the parallel data input/serial data input switch terminal.
P/S = “H”: Parallel data input.
P/S = “L”: Serial data input.
The following applies depending on the PS status:
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>“H”</td><td>A0</td><td>DB0 ~ DB7</td><td>/RD, /WR</td><td>X</td></tr>
<tr><td>“L”</td><td>A0</td><td>SI (DB7)</td><td>Write only</td><td>SCL (DB6)</td></tr>
</table>
When P/S = “L”, DB0 to DB5 fixed “H”.
/RD (EP) and /WR (RWP) are fixed to either “H” or “L”.
With serial data input, It is impossible read data from RAM .</td></tr>
<tr><td>4</td><td>C86</td><td></td><td>This is the MPU interface switch terminal.
C86 = “H”: 6800 Series MPU interface.
C86 = “L”: 8080 MPU interface.</td></tr>
<tr><td>5</td><td>VR</td><td></td><td>Output voltage regulator terminal. Provides the voltage between VDD and V5 through a resistive voltage divider. These are only enabled when the V5 voltage regulator internal resistors are not used (IRS = “L”). These cannot be used when the V5 voltage regulator internal resistors are used (IRS = “H”).</td></tr>
<tr><td>6</td><td>V0</td><td></td><td rowspan="5">This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on Vss, and must maintain the relative magnitudes shown below.
V0 ≧V1 ≧V2 ≧V3 ≧V4 ≧Vss
When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.
<table>
<tr><th></th><th>1/65 DUTY</th><th>1/49 DUTY</th><th>1/33 DUTY</th><th>1/55 DUTY</th><th>1/53 DUTY</th></tr>
<tr><td>V1</td><td>8/9*V0,6/7*V0</td><td>7/8*V0,5/6*V0</td><td>5/6*V0,4/5*V0</td><td>7/8*V0,5/6*V0</td><td>7/8*V0,5/6*V0</td></tr>
<tr><td>V2</td><td>7/9*V0,5/7*V0</td><td>6/8*V0,4/6*V0</td><td>4/6*V0,3/5*V0</td><td>6/8*V0,4/6*V0</td><td>6/8*V0,4/6*V0</td></tr>
<tr><td>V3</td><td>2/9*V0,2/7*V0</td><td>2/8*V0,2/6*V0</td><td>2/6*V0,2/5*V0</td><td>2/8*V0,2/6*V0</td><td>2/8*V0,2/6*V0</td></tr>
<tr><td>V4</td><td>1/9*V0,1/7*V0</td><td>1/8*V0,1/6*V0</td><td>1/6*V0,1/5*V0</td><td>1/8*V0,1/6*V0</td><td>1/8*V0,1/6*V0</td></tr>
</table></td></tr>
<tr><td>7</td><td>V1</td><td></td></tr>
<tr><td>8</td><td>V2</td><td></td></tr>
<tr><td>9</td><td>V3</td><td></td></tr>
<tr><td>10</td><td>V4</td><td></td></tr>
</table>

11	VRS		This is the internal-input VREG power supply for the lcd power supply
12	CAP4+		DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
13	CAP2-		DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.
14	CAP2+		DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
15	CAP1+		DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
16	CAP1-		DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.
17	CAP3+		DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal
18	CAP5+		DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
19	VOUT		DC/DC voltage converter. Connect a capacitor between this terminal and VSS
20	V_{SS}		Power Supply (VSS=0)
21	V_{DD}		Power Supply (VDD=3.0)
22	DB7		This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (PS = “L”), DB7 serves as the serial data input terminal (SI) and DB6 serves as the serial clock input terminal (SCL). At the same time, DB5 - 0 are set to high impedance. When the chip select is inactive, DB0 to DB7 are set to high impedance.
23	DB6		
24	DB5		
25	DB4		
26	DB3		
27	DB2		
28	DB1		
29	DB0		
30	/RD(E)		When connected to an 8080 MPU, this is LOW active. This pin is connected to the RD signal of the 8080 MPU, and the ST7565P series data bus is in an output status when this signal is “L”. When connected to a 6800 Series MPU , this is active HIGH. This is the 6800 Serier MPU enable clock input terminal.
31	/WR(RW)		When connected to an 8080 MPU, this is LOW active. This pin is connected to the RD signal of the 8080 MPU, and the ST7565P series data bus is in an output status when this signal is “L”. When connected to a 6800 Series MPU , this is active HIGH. This is the 6800 Serier MPU enable clock input terminal.

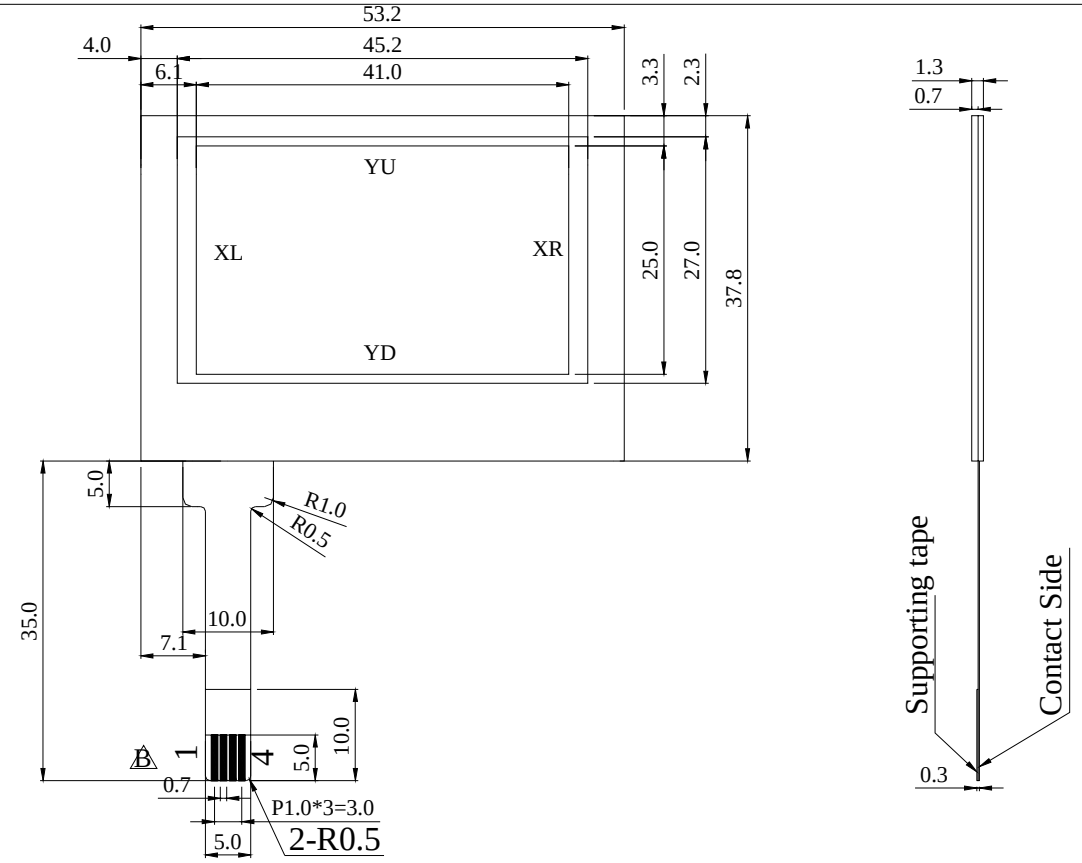
32	A0		This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = “H”: Indicates that DB0 to DB7 are display data. A0 = “L”: Indicates that DB0 to DB7 are control data.
33	/RES		/RES is set to “L”, the settings are initialized. The /RES signal level performs the reset operation.
34	/CS1		This is the chip select signal. When /CS1 = “L”, then the chip select becomes active, and data/command I/O is enabled.

Contour Drawing



PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	IRS	18	CAP5+
2	/HPM	19	VOUT
3	P/S	20	Vss
4	C86	21	VDD
5	VR	22	D7
6	V0	23	D6
7	V1	24	D5
8	V2	25	D4
9	V3	26	D3
10	V4	27	D2
11	VRS	28	D1
12	CAP4+	29	D0
13	CAP2-	30	/RD(E)
14	CAP2+	31	/WR(R/$\overline{W}$)
15	CAP1+	32	A0
16	CAP1-	33	/RES
17	CAP3+	34	/CS1

The non-specified tolerance of dimension is ±0.2mm.



PIN OUT	
1	YU
2	XL
3	YD
4	XR

The non-specified tolerance of dimension is ±0.2mm.