Winstar Display Co., LTD
華凌光電股份有限公司
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SPECIFICATION

CUSTOMER : _____

MODULE NO.: WO12864-05GC2#FC

APPROVED BY: (FOR CUSTOMER USE ONLY)	PCB VERSION: DATA:

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
first FC components			

VERSION	DATE	REVISED PAGE NO.	SUMMARY
B	2014/04/25		Remove IC information

General Specification

Item	Dimension	Unit
Number of Characters	128 x 64 dots	—
Module dimension	53.2 x 37.8 x 2.0(MAX)	mm
View area	45.2 x 27.0	mm
Active area	40.92 x 24.28	mm
Dot size	0.28 x 0.34	mm
Dot pitch	0.32 x 0.38	mm
LCD type	FSTN Positive Reflective (In LCD production, It will occur slightly color difference. We can only guarantee the same color in the same batch.)	
Duty	1/64 , 1/9 Bias	
View direction	6 o'clock	
Backlight Type	Without backlight	
IC	ST7565P	

Absolute Maximum Ratings

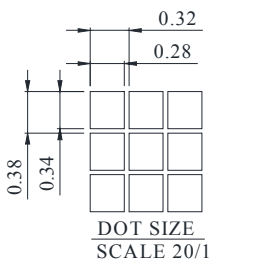
Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20	—	+70	℃
Storage Temperature	T_{ST}	-30	—	+80	℃
Power Supply Voltage	VDD	-0.3	—	3.6	V
Power supply voltage (VDD standard)	V0, VOUT	-0.3	—	14.5	V
Power supply voltage (VDD standard)	V1, V2, V3, V4	-0.3	—	V0+0.3	V

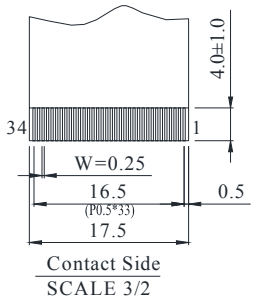
Interface Pin Function

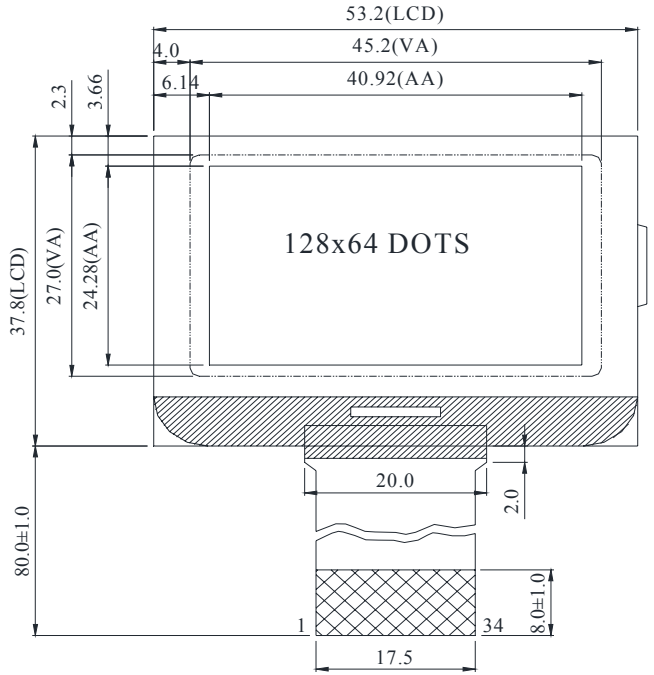
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Level</th><th>Description</th></tr>
<tr><td>1</td><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V0 voltage level adjustment.
IRS = “H”: Use the internal resistors
IRS = “L”: Do not use the internal resistors. The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal</td></tr>
<tr><td>2</td><td>/HPM</td><td>I</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
/HPM = “H”: Normal mode
/HPM = “L”: High power mode</td></tr>
<tr><td>3</td><td>P/S</td><td>I</td><td>This is the parallel data input/serial data input switch terminal.
P/S = “H”: Parallel data input.
P/S = “L”: Serial data input.
The following applies depending on the P/S status:
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>“H”</td><td>A0</td><td>D0 to D7</td><td>/RD, /WR</td><td>X</td></tr>
<tr><td>“L”</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr>
</table>
When P/S = “L”, D0 to D5 fixed “H”.
/RD (E) and /WR (R/W) are fixed to either “H” or “L”.
With serial data input, It is impossible read data from RAM</td></tr>
<tr><td>4</td><td>C86</td><td>I</td><td>This is the MPU interface selection pin.
C86 = “H”: 6800 Series MPU interface.
C86 = “L”: 8080 Series MPU interface</td></tr>
<tr><td>5</td><td>VR</td><td>I</td><td>Output voltage regulator terminal. Provides the voltage between VSS and V0 through a resistive voltage divider.
IRS = “L” : the V0 voltage regulator internal resistors are not used.
IRS = “H” : the V0 voltage regulator internal resistors are used.</td></tr>
<tr><td>6~10</td><td>V0~V4</td><td>Power Supply</td><td>This is a multi-level power supply for the liquid crystal drive.</td></tr>
<tr><td>11</td><td>VRS</td><td>Power Supply</td><td>This is the internal-output VREG power supply for the LCD power supply voltage regulator.</td></tr>
<tr><td>12</td><td>CAP4+</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.</td></tr>
</table>

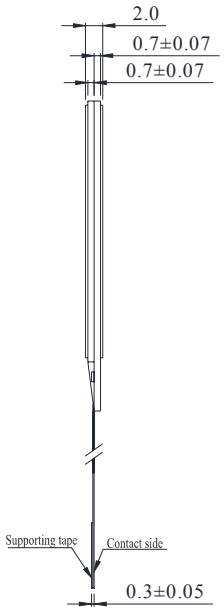
13	CAP2-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.
14	CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.
15	CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
16	CAP1-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.
17	CAP3+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
18	CAP5+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
19	VOUT	O	DC/DC voltage converter. Connect a capacitor between this terminal and vss or VDD
20	VSS	Power Supply	Ground
21	VDD	Power Supply	Power supply
22~29	D7~D0	I/O	Data bus line
30	/RD(E)	I	• When connected to 8080 series MPU, this pin is treated as the "/RD" signal of the 8080 MPU and is LOW-active. The data bus is in an output status when this signal is "L". • When connected to 6800 series MPU, this pin is treated as the "E" signal of the 6800 MPU and is HIGH-active. This is the enable clock input terminal of the 6800 Series MPU.
31	/WR(RW)	I	• When connected to 8080 series MPU, this pin is treated as the "/WR" signal of the 8080 MPU and is LOW-active. The signals on the data bus are latched at the rising edge of the /WR signal. • When connected to 6800 series MPU, this pin is treated as the "R/W" signal of the 6800 MPU and decides the access type : When R/W = "H": Read. When R/W = "L": Write.
32	A0	I	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.
33	/RES	I	When RES is set to "L", the setting are initialized.
34	/CS1	I	This is the chip select signal.

Contour Drawing









PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	IRS	18	CAP5+
2	/HPM	19	VOUT
3	P/S	20	Vss
4	C86	21	VDD
5	VR	22	D7
6	V0	23	D6
7	V1	24	D5
8	V2	25	D4
9	V3	26	D3
10	V4	27	D2
11	VRS	28	D1
12	CAP4+	29	D0
13	CAP2-	30	/RD(E)
14	CAP2+	31	/WR(R/$\overline{W}$)
15	CAP1+	32	A0
16	CAP1-	33	/RES
17	CAP3+	34	/CS1

The non-specified tolerance of dimension is ±0.2mm.