Next Vision Display
Brighten The Future

NEXT VISION DISPLAY

SPECIFICATION

CUSTOMER : _____

MODULE NO.: NVE154-200200BSM090#GD

Version	2.1
Engineer	
Date	2020/07/09

Customer:
Approved by

NEXT VISION DISPLAY CO., LTD.

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General Description

Over View

The display is a TFT active matrix electrophoretic display, with interface and a reference system design. The 1.54" active area contains 200×200 pixels, and has 1-bit white/black full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border are supplied with each panel.

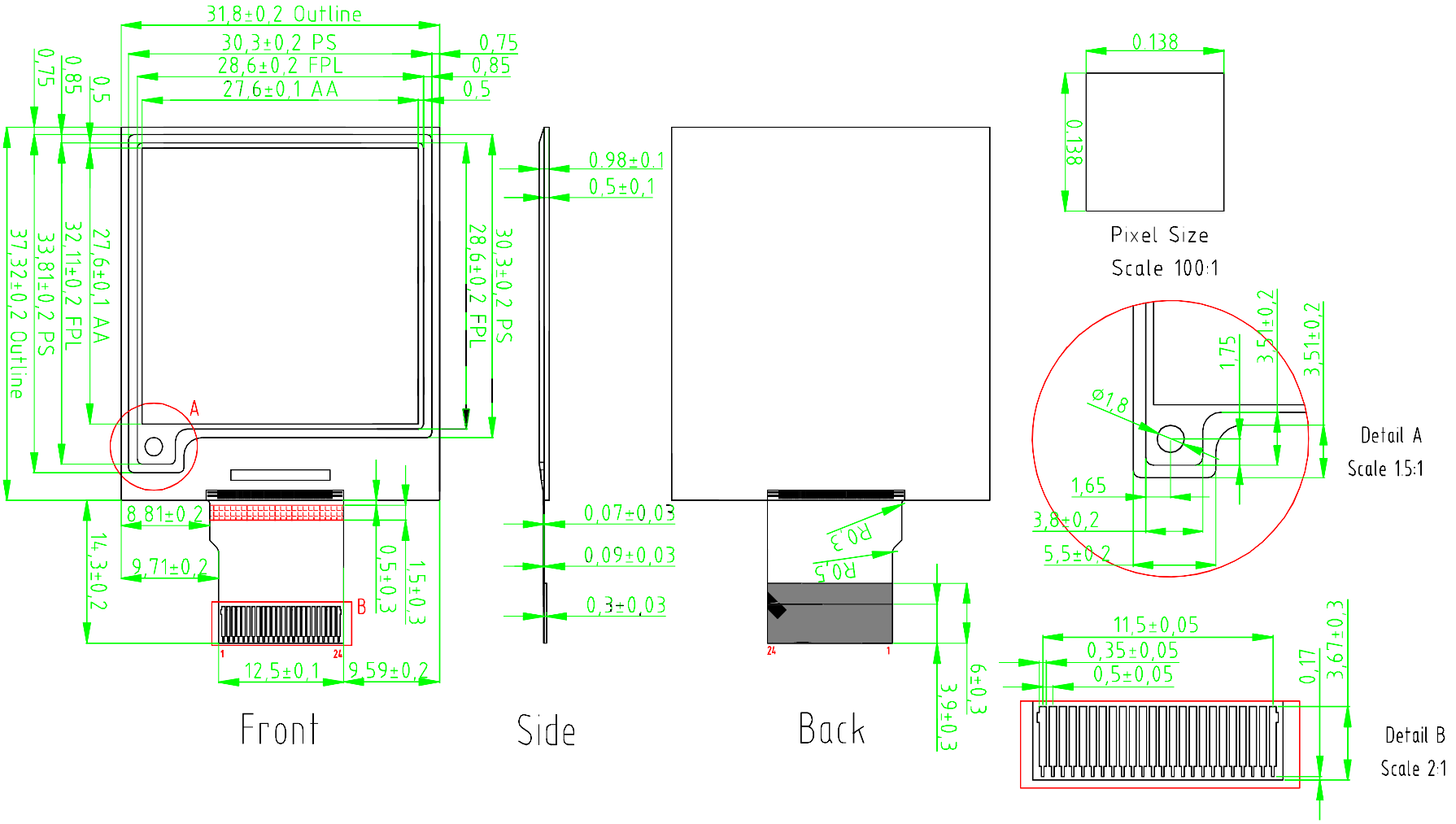
Features

- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and source driving voltage
- I^2C Signal Master Interface to read external temperature sensor
- Available in COG package IC thickness 230um

Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	1.54	Inch	
Display Resolution	200(H)×200(V)	Pixel	Dpi:184
Active Area	27.6(H)×27.6(V)	mm	
Pixel Pitch	0.138×0.138	mm	
Pixel Configuration	Square		
Outline Dimension	31.80(H)×37.32(V) ×0.98(D)	mm	
Weight	2.5±0.5	g	

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It is forbidden to copy or disclose the information without the written authorization



Note:

1. Resolution:200(G)*200(S)
2. DPI:184
3. Unlabeled tolerances:±0.15

					File Serial Number: NVE154-200200BSM090#GD
MARK:	CHANGE CONTENT		SIGNATURE	DATE	WF P/N:
DRAWN:		TECHNOLOGY:			SCALE: 1:1 / SIZE: mm / Material:
PROOF-READ		CHECKED:			Version Number: / Publish Date:
STANDARDIZATION		APPROVALS:			SHEET 1 OF 1

Input/Output Terminals

Pin out List

Pin #	Type	Single	Description	Remark
1		NC	No connection and do not connect with other NC pins	Keep Open
2	O	GDR	N-Channel MOSFET Gate Drive Control	
3	O	RESE	Current Sense Input for the Control Loop	
4	C	VGL	Negative Gate driving voltage	
5	C	VGH	Positive Gate driving voltage	
6	O	TSCL	I^2C Interface to digital temperature sensor Clock pin	
7	I/O	TSDA	I^2C Interface to digital temperature sensor Date pin	
8	I	BS1	Bus selection pin	Note 1.5-5
9	O	BUSY	Busy state output pin	Note 1.5-4
10	I	RES #	Reset	Note 1.5-3
11	I	D/C #	Data /Command control pin	Note 1.5-2
12	I	CS #	Chip Select input pin	Note 1.5-1
13	I/O	D0	serial clock pin (SPI)	
14	I/O	D1	serial data pin (SPI)	
15	I	VDDIO	Power for interface logic pins	
16	I	VCI	Power Supply pin for the chip	
17		VSS	Ground	
18	C	VDD	Core logic power pin	
19	C	VPP	Power Supply for OTP Programming	
20	C	VSH	Positive Source driving voltage	
21	C	PREVGH	Power Supply pin for VGH and VSH	
22	C	VSL	Negative Source driving voltage	
23	C	PREVGL	Power Supply pin for VCOM, VGL and VSL	
24	C	VCOM	VCOM driving voltage	

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active Low.

Note 5-4: This pin (BUSY) is Busy state output pin. When Busy is low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin low when the driver IC is working such as:

- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI(9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI

Reference Circuit

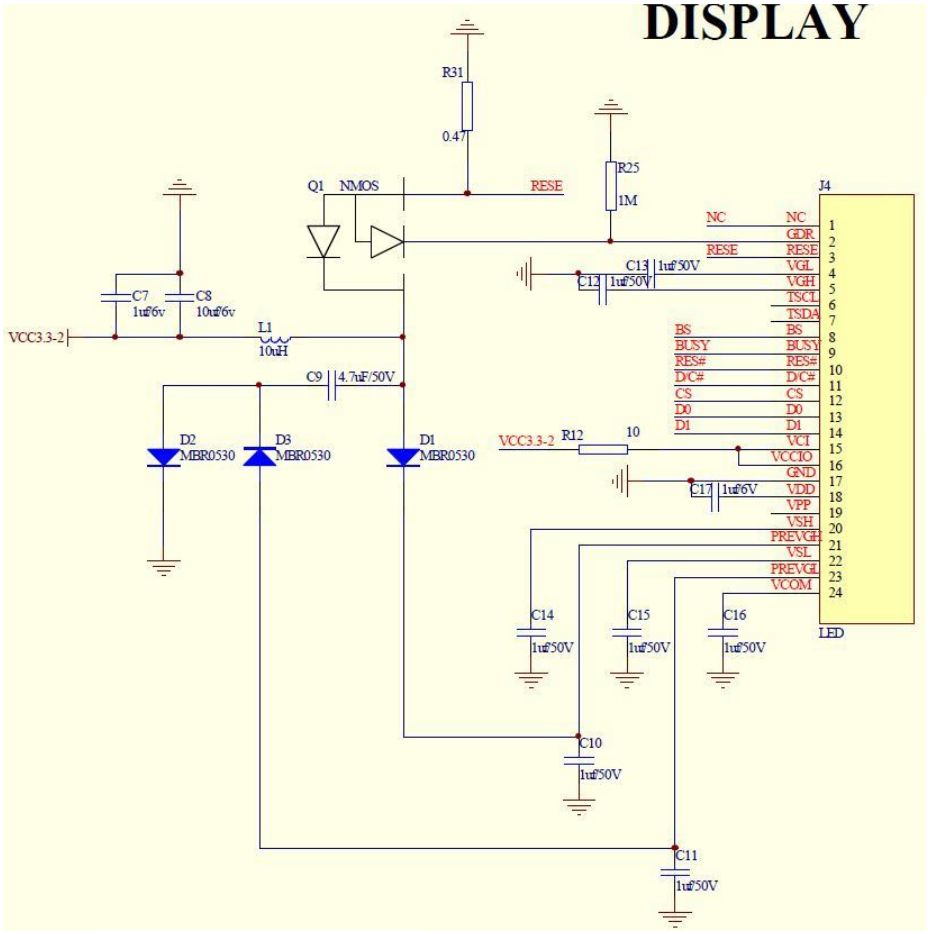


Figure . 1.6-5 (1)

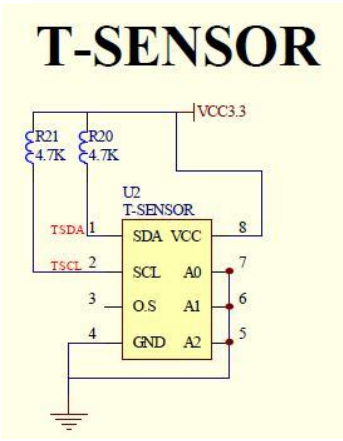


Figure . 1.6-5 (2)